Happy holidays! from all of us at Imperas, and thanks for your support in making 2018 a record-breaking year.

We have experienced great growth in the adoption of virtual platforms, plus Verification, Analysis, Profiling (VAP) tools for software development, driven notably by:

- The industry momentum in custom SoC designs requiring heterogeneous processor support.
- The adoption of Imperas simulation technology as a reference for the RISC-V Foundation Compliance task group with riscvOVPsim.
- Our many partnerships, including Arm, MIPS, UltraSoC, Andes, Valtrix, Arc, Cadence, Mentor, the prpl Foundation, SafePower, TV&S, Xilinx, and Magillem, plus other partners and projects we are yet to announce in detail.
- Our distributors: eSOL Trinity (Japan), Coontec (Korea) and our latest addition QLS (Quantum Leap Sales) for North America.
- Customer projects in areas of automotive, industrial, mobile and security-related embedded systems and software.

We also welcome our newest customers and users, some of which are CEA, Palfinger, Samsung, and Coca-Cola, together with new academic users including Pusan National University, Eindhoven University of Technology, National Cheng Kung University, Loughborough University, Katholieke Universiteit Leuven, ETH Zurich, University of Bristol, and Boise State University.

In 2019, we will be delivering more: more of the fastest processor models; more tools for software development, debug and test; and more expansion of the Imperas ecosystem.

We look forward to continuing to work with you! Please follow Imperas on LinkedIn, twitter @ImperasSoftware and YouTube.
TECHNOLOGY HIGHLIGHTS

**Imperas Empowers RISC-V Community with riscvOVPsim** November 2018

- See the Video Demo and Introduction to riscvOVPsim
- See RISC-V Solutions on Imperas website

**RISC-V RV64GC High-Performance Extendable Platform Kit For Fast Linux Execution Released by Imperas** February 2018

EVENTS

- **Andes RISC-V Con in Beijing and Silicon Valley** November 2018
- **RISC-V Panel at Electronica** November 2018
- **RISC-V Cambridge Meetup with UltraSoC** October 2018
- **Inaugural RISC-V Summit, Santa Clara** December 2018
- **RISC-V Bristol Meetup hosted by UltraSoC** October 2018
- **Arm TechCon 2018 San Jose** October 2018
- **DVCon Europe 2018 Munich** October 2018
- **RISC-V Day Tokyo** October 2018
- **June RISC-V Bay Area Meetup** June 2018
- **DAC 2018 in San Francisco** June 2018
- **RISC-V Workshop Barcelona** May 2018
- **IoT/M2M Expo in Tokyo (eSOL TRINITY)** May 2018
- **RISC-V Chennai India** July 2018
- **DATE in Germany, Dresden** March 2018
- **Automotive Testing Expo in Korea (Coontec)** March 2018
- **Embedded World Exhibition and Conference, Nuremberg** February 2018

CORPORATE AND PARTNERSHIP HIGHLIGHTS

- **Imperas expands commercial operations with Quantum Leap Sales for US market growth** December 2018
- **Imperas and Valtrix announce partnership for RISC-V Processor Verification** December 2018
- **Andes Certifies Imperas Models and Simulator as a Reference for Andes RISC-V Cores** June 2018
- **UltraSoC embedded analytics and Imperas virtual platforms combine to enhance multicore development and debug** June 2018
- **Imperas and Andes Extend Partnership, Delivering Models and Virtual Platforms for Andes RISC-V Cores with New AndeStar V5m Extensions** May 2018
- **Imperas Appoints Kevin McDermott as Vice President of Marketing** March 2018
- **Ashling and Imperas Partner to Extend the RISC-V Ecosystem** February 2018
- **Magillem Partners with Imperas** February 2018

IN THE NEWS: ARTICLES AND BLOGS

- **Imperas and RISC-V: SemiWiki** December 6 2018
- **RISC-V shines at DVCon Europe: DVCon Europe Imperas guest blog with UltraSoC** November 9 2018
- **Imperas’ riscvOVPsim gives RISC-V Community a Boost: Embedded Computing by Laura Dolan** November 6 2018
- **UltraSoC announces integrated multi-core debug, visualization and data science / analytics suite, with Imperas** October 16 2018
- **RISC-V: More than a Core: Semiconductor Engineering by Brian Bailey** October 15 2018
- **Experts Examine New Innovations and Share Advice for Future Engineers: ECN Roundtable Part 2**
VIDEOS

Video at RISC-V 2018 Summit: Simon Davidmann presenting RISC-V Compliance in the Era of Open ISA and Custom Instructions
Imperas EDA Café video: Interview with Simon Davidmann, CEO of Imperas Software at ARM TechCon 2018.
Andes DevCon RISC-V panel with Larry Lapides.
riscvOVPsim introduction with Simon Davidmann
riscvOVPsim. A complete RISC-V ISS for bare-metal software development and Specification Compliance Test Development
RISC-V Custom Instruction Design and Verification Flow
Software Development Methodology for RISC-V Devices with RTOS and Linux or Both
Imperas at Embedded World 2018: Rich Nass interviews Larry Lapides
The Challenge of Systemic Complexity - EE Journal - Amelia Dalton
See new Imperas demos here.

IMPERAS UNIVERSITY PROGRAM HIGHLIGHTS

Universite Bretagne Loire: Used Imperas simulation on the TUSUNAMY project supported by the Agence Nationale de la Recherche (ANR) addresses the problem of secure handling of personal data and privacy in many-core architectures.
FAU (Erlangen-Nuremberg) As part of the Research Training Group “heterogeneous image systems”, developing a processor model for the Epiphany Many Core CPU.
University of Nantes: Application Deployment Strategies for Spatial Isolation on Many-core Accelerators.
UFRGS (Universidade Federal do Rio Grande do Sul) and Loughborough University: A Fault-Injection Tool for Detailed and Efficient Multicore Soft Error Vulnerability Analysis.

OVP RELEASE NEWS


A new Imperas and OVP release became available November 2018. The Open Virtual Platforms portal is one of the most exciting open source software developments in the embedded software world since GNU created GDB.
For embedded software developers, virtual platforms are increasingly important, especially for multi-core designs.

The resources on this portal can significantly accelerate your development and test.