



RISC-V Reference Model for Processor DV

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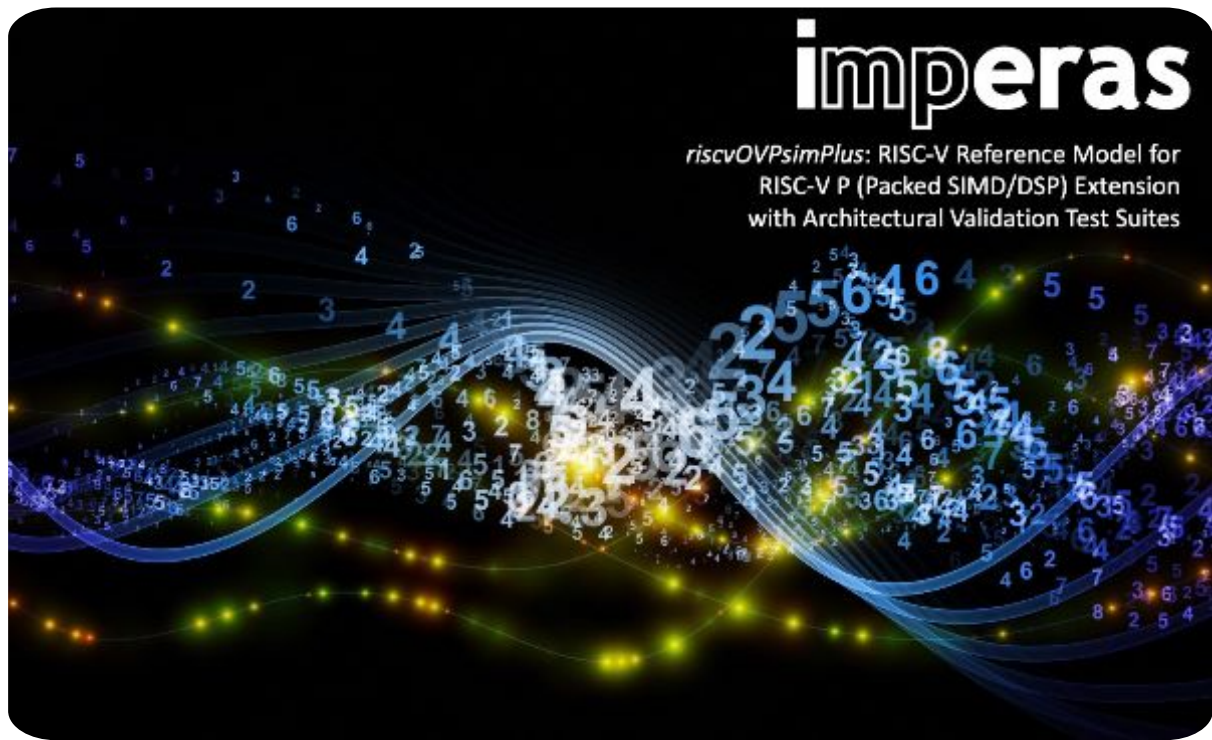


Imperas simulation technology and RISC-V reference models updated to cover the RISC-V P Extension for SoC architecture exploration and early software development.

“RISC-V is more than an ISA specification, it is a framework of flexibility; the real value is in the extensions and options available for processor core implementations,” said **Dr. Charlie Su, President and CTO at Andes Technology Corp.** “The RISC-V P extension within the Andes cores addresses the key real-time requirements in SIMD/DSP computations for new markets in audio/speech, IoT, tinyML and edge devices. Together with the Andes certified Imperas reference models, SoC developers can explore the next generation domain-specific solutions.”

“Embedded development depends on the optimized balance between hardware resources and software applications,” said **Simon Davidmann, CEO at Imperas Software Ltd.** “With the Imperas golden reference models, developers can explore full software development for all the Andes cores, including the new RISC-V P extension and Andes ACE custom instructions.”

For more information, please [click here](#).



Imperas simulation technology and reference model is available for free, including test suites for basic processor hardware verification and compliance testing.

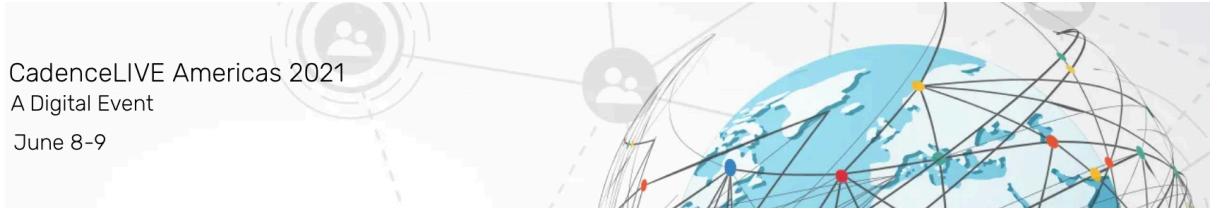
“Flexibility within a framework of compatibility is the essential foundation of the RISC-V ISA,” said **Chuanhua Chang, Andes Technology Corporation, Chair of RISC-V International P Extension Task Group**. “The RISC-V P extension defines a rich set of integer SIMD/DSP instructions operating on existing integer registers to support complex data processing within the constraints of real-time applications. However, the hardware specification is just the start - adoption and success depend on the software ecosystem, which is supported with the reference models and test suites from Imperas.”

“By combining SIMD/DSP functionality within the RISC-V ISA offers the ideal balance for performance, flexibility and efficiency,” said **Wei Wu, PLCT Lab, ISCAS, Vice-Chair of RISC-V International P Extension Task Group**. “The Imperas RISC-V reference model provides the ideal starting point to explore and develop software algorithms based on the new RISC-V P extension.”

“The Imperas simulation technology and RISC-V reference models are in active use in some of the most complex RISC-V verification projects,” said **Simon Davidmann, CEO at Imperas Software Ltd**. “RISC-V is changing the design process as new design exploration can start without many of the traditional barriers. The adoption of [riscvOVPsimPlus](#) with the new RISC-V P extension support helps provide clarification of the specification boundary as a useful guideline for innovation in new processor designs.”

For more information, please [click here](#).

Events



CadenceLIVE Americas 2021
A Digital Event
June 8-9

If you missed the CadenceLIVE Americas conference or registered but didn't manage to watch all of the sessions, it's now available [on-demand](#). Registration is free; once registered navigate yourself to the talks from the main lobby.

During the conference, we delivered two technical presentations on the latest advances for RISC-V verification.

[The Step-and-Compare methodology for high quality RISC-V processor verification](#)

Co-author: ***Simon Davidmann***, Imperas Software

Co-author: ***Lee Moore***, Imperas Software

This talk, which is under the verification section in the agenda, introduces the various options for RISC-V processor verification from the simple trace analysis through to the latest techniques with test benches that support UVM SystemVerilog with Step-and-Compare for asynchronous events. With illustration of the various options and approaches including details of bugs found on some popular open-source cores.

[The open verification method used by OpenHW for the CV32E40P RISC-V core](#)

Co-author: ***Mike Thompson***, OpenHW Group

Co-author: ***Lee Moore***, Imperas Software

This talk, which is under the IP section in the agenda, explores the background, development and implementation of the OpenHW verification environment for CV32E40P known as “core-v-verif”. Since the goal of the project is to support the adoption of an open-source core, the initial deliverable quality is not the only concern. One attractive aspect of an open-source core is the potential for adopters to modify, adapt, or extend the base core features. Thus, the verification plan needs to anticipate the future use case with flexibility built-in and clear documentation for the full test bench to be adopted and further adapted by end-users.



At the recent [RISC-V Forum on Security](#), we presented an introduction to the open-source Architectural Validation tests for RISC-V Crypto “K”. The new scalar cryptography extension for RISC-V is designed to be lightweight and is suitable for 32- & 64-bit base architectures, from embedded, IoT class cores to large, application class cores. The Architectural Validation Test Suites help RISC-V developers test the implementations are in-line with the specifications.

[Getting started with Architectural Validation tests for RISC-V Crypto “K”](#)

Speaker: *Simon Davidmann, Imperas Software*

This talk is [available online](#) and covers the use of the open-source Crypto architectural validation test suites as part of a RISC-V processor test pan, including the key resources and setup guides.

ARTICLES FROM



SEMICONDUCTOR ENGINEERING
DEEP INSIGHTS FOR THE TECH INDUSTRY

[Debug: The Schedule Killer](#)

Debug often has been labeled the curse of management and schedules. It is considered unpredictable and often can happen close to the end of the development cycle, or even after – leading to frantic attempts at work-arounds. And the problem is growing...

To read the full article by **Brian Bailey**, [click here](#).

Data Centers On Wheels

Automotive architectures are evolving quickly from domain-based to zonal, leveraging the same kind of high-performance computing now found in data centers to make split-second decisions on the road.

To read the full article by **Ann Steffora Mutschler**, [click here](#).

Rocky Road To Designing Chips In The Cloud

As EDA is moving to the cloud in fits and starts as tool vendors sort out complex financial models and tradeoffs while recognizing a potentially big new opportunity to provide unlimited processing capacity using a pay-as-you-go approach.

To read the full article by **Ann Steffora Mutschler**, [click here](#).



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on Semiconductor Engineering

RISC-V:

The 5 levels of simulation-based processor hardware design verification

RISC-V is enabling processor design freedoms to the broad community of SoC developers, but this also represents a migration of the processor design verification task from the teams at a few mainstream IP providers to all RISC-V adopters. Developers that accept the design freedoms of RISC-V must also undertake the appropriate level of verification responsibility.

In some cases, a simple comparison-based trace analysis is sufficient to confirm some level of basic operation of the processor, while designs targeted at volume production and/or high-reliability applications will justify significant additional verification efforts. The challenge of RISC-V is not just the verification task, but the correct selection of the quality level appropriate for the end application.

To read the article in full, [click here](#).

Release Information

OVP and riscvOVPsim RELEASE NEWS

The latest Imperas and OVP release at the [Open Virtual Platforms website](#).



For an introduction to RISC-V the free single core envelope model, called **riscvOVPSim**, is an excellent starting point, which can be configured for all the ratified ISA features and includes support of the draft specifications for Bit Manipulation and Vectors.

The latest version was is available via [GitHub here](#).

The free enhanced **riscvOVPSimPlus**, including many more features including full configurable instruction trace, GDB/Eclipse debug, and memory configuration options, plus the RISC-V Vector and other test suites, is now available on the [OVP website here](#).

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