Open-Source RISC-V Cores with Industrial Strength Verification

RISC-V Summit

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Agenda

• Background of OpenHW
• Evolution of ‘core-v-verif’ core verification environment
• Case Study demonstration
• Components of Industrial Strength DV
  • Adoption of standards
• Summary
• Global, Non Profit based in Canada, Founded by Rick O’Connor, founding Executive Director of RISC-V Foundation
• Focus: develop open source cores with industrial quality verification
• Founded late 2019, 80+ member companies, 10+ partners
• Original cores evolved from the ‘RI5CY’ range developed at PULPplatform / ETH Zurich
• Currently 9 RISC-V cores under development
  • 32bit, 64bit, controller/application, bare metal/Linux, etc.
• Developed quality DV testbench and flows: ‘core-v-verif’
• Imperas partners providing ‘golden reference’ RISC-V models & DV technology
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OpenHW ‘core-v-verif’

- Provides a robust, comprehensive simulation environment for the cores:
  - RISC-V 32bit: CV32E40P, CV32E40X, CV32E40S, CV32A6, ...
  - RISC-V 64bit: CV64A6, ...
- Freely available on github at openhwgroup/core-v-verif
- Industrial-strength verification
  - SystemVerilog UVM environment
  - Runs on any commercial SystemVerilog-compatible simulator
  - Complete code coverage
  - Well-defined comprehensive functional coverage
  - Open and complete verification plans for each core
‘core-v-verif’ in 2020

- Runs core RTL and Imperas reference model co-sim
- Includes sync and async lock-step-compare
- For interrupts and debug includes
  - random stimulus
  - properties and assertions
  - functional coverage
- Uses directed and constrained random tests
- Encapsulation of Imperas OVP reference model in SystemVerilog
- Challenge was support for many different cores
‘core-v-verif’ in 2021 – evolution to using standards

Use bespoke tracer+control, (RVFI) for Interface to DUT RTL

Use RVVI for Interface to Imperas reference Model

RISCV Core (DUT)

Tracer (RVFI) (*)

Control

Testbench, control, sequencing, comparing, scoreboard (SystemVerilog)

RVVI

RISCV Imperas reference Model

(*) RVFI code is used as base for the DUT tracer/streaming i/f - has extensions as required
RVVI is new developing open standard (RISC-V Verification Interface) (more on later slides)
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Imperas is the Reference Model & Simulator

- Imperas provides full RISC-V Specification envelope model
- Industrial quality model /simulator of RISC-V processors for use in compliance, verification and test development
- Complete, fully functional, configurable model / simulator
  - All 32bit and 64bit features of ratified User and Privilege RISC-V specs
  - Vector extension, versions 0.7.1, 0.8, 0.9, 1.0
  - Bit Manipulation extension, versions 0.91, 0.92, 0.93, 1.0.0
  - Hypervisor version 0.6.1
  - K-Crypto Scalar version 0.7.1, 1.0.0
  - Debug versions 0.13.2, 0.14, 1.0.0
- Model source included under Apache 2.0 open source license
- Used as reference by:
  - Mellanox/Nvidia, Seagate, NSITEXE/Denso, Google Cloud, Chips Alliance, lowRISC, OpenHW Group, Andes, Valtrix, SiFive, Codasip, MIPS, Nagra/Kudelski, Silicon Labs, RISC-V Compliance Working Group, ...

Imperas is used as RISC-V Golden Reference Model
Reference Model Encapsulation

BIU (Fetch, Load/Store)
Async Events
Interrupts
Debug

Code
Data

SV - DPI Wrapper
Reference Model
Custom Ext

State

GPR
CSR
MODE
DEBUG

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Reference Model Debug / Analysis Capabilities

- **BIU (Fetch, Load/Store)**
- **Code**
- **Data**
- **SV - DPI Wrapper**
- **Custom Ext**
- **Async Events**
- **Interrupts**
- **Debug**
- **State**

**RTL Debug**

**S/W Debug**

**S/W Trace**

**S/W Analysis**

**Capabilities**

- Reference Model Debug / Analysis
- BIU (Fetch, Load/Store)
- Code
- Data
- SV - DPI Wrapper
- Custom Ext
- Async Events
- Interrupts
- Debug
- State
- GPR
- CSR
- MODE
- DEBUG
OpenHW cv32e40p Step/Compare
UVM Testbench

make test SIM=<simulator> TEST=<test_case>

Compiler Toolchain

testcase.S

GCC compile elf2hex

Functional Coverage

SV - DPI Wrapper

Golden ISS Reference Model

Compare all CSRs, GPRs and PC

Step & Compare

SVA

CV RTL

Compiler Toolchain

vp

dp_ram

mm_ram

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DRAFT

- Run fail
- Run with pass

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Components of Industrial Strength DV

- Functional coverage measurement
- (random) Instruction test generator
- Testharness control, sequencing, compare (SystemVerilog, C or C++)
- Imperas DV subsystem
- Encapsulation of Imperas reference model

NOTE: ImperasDV can be used with SystemVerilog, C, C++, Verilator

5 components of RISCV CPU DV
- (random) instruction test generator
- DUT subsystem
- Functional coverage measurement
- Test bench / harness
- Imperas DV subsystem
Evolving RVVI: RISC-V Verification Interface
(3 components, public open standard)
[driven by RISC-V DV usage]

- https://github.com/riscv-verification/RVVI
- RVVI-VLG
  - 4 SystemVerilog Interfaces
    - RVVI_state
    - RVVI_control
    - RVVI_io (Interrupts, Debug)
    - RVVI_bus -(Data, Instruction Bus)
- RVVI-API
  - C/C++
  - SystemVerilog
- RVVI-VPI (work-in-progress)
  - Virtual Peripheral Interfaces
    - timers, interrupts, debug, random, printer/uart, ...
  - Verilog and C macros & examples
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Summary

- RISC-V processor DV needs lock-step-compare to be of high quality
  - Lock-step is the only way to verify asynchronous behaviors
- Need standards like RVVI to allow component reuse to be efficient
  - For have several different cores, or evolving generations
- Openhw core-v-verif is a high quality test bench
  - Open source means you can clone and use it if you modify / extend the OpenHW cores
  - And also you can make use of it or its components in your test benches for other cores
- Imperas is used as key technology in terms of reference model and DV
  - All you need for high quality, cost-effective RISC-V processor DV... come talk to us
- Imperas: used as a reference by:
  - Mellanox/Nvidia, Seagate, NSITEXE/Denso, Google Cloud, Chips Alliance, lowRISC, OpenHW Group, Andes, Valtrix, SiFive, Codasip, MIPS, Nagra/Kudelski, Silicon Labs, RISC-V Compliance Working Group, ...
Thank you

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