Is hardware/software co-design now a reality for applications with RISC-V?

Kevin McDermott, 8\textsuperscript{th} December 2021
Announcing a new era of integrated electronics

A micro-programmable computer on a chip!

The original November 15, 1971 ad for the Intel 4004. 

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Microprocessor timeline (the first 50 years)

- Computer on a chip
- The RISC vs CISC wars
  - Can complexity help simplify the problem
- Desktop and embedded
  - Complexity and quality, embedded reliability for critical systems
- Supercomputer (Academic) -> Datacenter (Commercial)
  - Lots of compute resources, some cost/size/location implications
- Standard devices vs Application Specific Integrated Circuits (ASIC’s)
  - Design for the mass market or optimize systems performance at the chip level
- Multicore & SoC (System on Chip)
  - Heterogeneous, just the right features in just the right configuration
  - 10’s, 100’s, 1,000’s of cores........
And do not forget about the software.....

- Programming languages
- Development tools
- Operating Systems and RTOS (Real-Time Operating System)
- Application software
- Internet
- Apps
- Games
“nobody designs a chip without simulation”, at Imperas we believe that:

“nobody should develop embedded software without simulation”

Imperas develops simulators, tools, debuggers, modeling technology, and models to help embedded systems developers and SoC designers get their systems running... and their hardware verified.

12+ years, self funded, profitable, UK based, team with much EDA (simulators, verification), processors, and embedded experience.

www.imperas.com  www.OVPworld.org
Simulation solutions for SW developers

- World class multicore simulator and full system emulator
- Library of advanced Verification, Analysis, Profiling tools
- Eclipse based Multiprocessor / Multicore debugger
• New solution to make it easy to verify RISC-V processor
• Works with SystemVerilog or C/C++ and Verilator
• sync-lock-step-compare and async-lock-step-compare
• This demo is RISC-V RV32, also runs on Imperas: RV32,RV64,MIPS32,ARM32,ARM64,OR1K
• Imperas virtual platform simulators can do sound, mouse/keyboard input, graphics output
• Imperas runs fast, real-time or faster...
Co-Design: HW and SW
Optimistic view of optimized design flow

The ideal goal:

• Hardware optimized for the application requirements
• Software optimized for the hardware resources and efficiency
  • Repeat above steps.....

But what about the iteration time.....

• Hardware prototypes based on 1st order assumptions => estimate (guess ?)
  • Software partitioned for anticipated resources that are not yet implemented
    • Wait for hardware availability, wait to test full application, wait to debug....
    • Wait for software to test the prototype hardware (see step #1)
      • Slow iteration cycles => latest hardware runs last generation software a bit better
Amdahl’s Law - A guideline for multi-core efficiency

- IBM computer architect & entrepreneur
  - Left IBM when his ideas were rejected
  - Founded Amdahl computers:
    - Cheaper, faster, more reliable
    - IBM plug-compatible...
- Amdahl’s law (1967) is used in parallel computing to predict the theoretical speedup when using multiple processors

\[ S_{\text{latency}}(s) = \frac{1}{(1 - p)} + \frac{p}{s} \]

- \( S_{\text{latency}} \) is the theoretical speedup of the execution of the whole task;
- \( s \) is the speedup of the part of the task that benefits from improved system resources;
- \( p \) is the portion of execution time that the part benefiting from improved resources originally occupied.
Why RISC-V?

• Optimized processor
  • Just the right features with just the right configuration
  • Flexible but standard extensions (= software ecosystem support)
  • Custom instructions (= application optimizations)

• Optimized platforms
  • Heterogeneous from multcore to clusters and beyond
  • Multiple optimized processors within a common framework
  • Custom hardware design with software compatibility
Modern Application Development Example for AI hardware accelerators

• Cloud based resources
  • Develop AI algorithm
  • Real word datasets (large scale models)
  • Need hardware acceleration for efficiency and deployment

• Virtual Prototype
  • Model hardware as abstraction for software development
  • Iterate design configurations at the speed of software
  • Functional test framework for processor hardware
  • SW and HW co-design
Example customer project

- Customer project
  - Full AI / ML engine
  - 150+ CPU cores
    - Over half with RISC-V Vector extension engine
- Imperas Reference Models and Virtual Platform provides environment for software stack development
- Simulation runs of software stack running in virtual platform take ~ 2hrs @ 500MIPS
  - Cross compiled software running on simulated CPUs
- Allows hardware platform configuration, re-configuration, architectural changes
  - Explore performance options
  - Runs real software (production binaries) – can see how it interacts with HW configuration
- Running in Imperas virtual prototype more than a year before RTL commit
  - Customer has SW and is looking to design HW to make it work the way they want...
- Also a by-product: kick-start SoC process by feeding models into HW DV at start
RISC-V => Freedom to innovate

• Design options now available at the point of use
  • End of the ‘one-size-fits-all’
  • Optimize with the right features and configuration options

• With RISC-V any developer can now optimize a custom processor
  • If you design it, you also need to test it!

  • Processor verification is migrating from a few specialist IP suppliers to all IP users that customize or optimize a RISC-V processor
ImperasDV for RISC-V CPU Verification

5 components of RISCV CPU DV
- (random) instruction test generator
- DUT subsystem
- Functional coverage measurement
- Test bench / harness
- Imperas DV subsystem

NOTE: ImperasDV can be used with SystemVerilog, C, C++, Verilator

Encapsulation of Imperas reference model
RISC-V leading the next X years of Processors

- Open standard ISA
- Standard extensions and configurations
- Extensive software ecosystem support
- Flexibility with Compatibility

- Optimized hardware with software co-design
  - Start your next project with Virtual Prototypes
    - Why wait for hardware?

- 2022 prediction
  - Verification ecosystem supports mass adoption of RISC-V innovation
Thank you!

Stop by our booth in the RISC-V exhibit area or contact us at

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