New Ecosystem Leads RISC-V Mainstream Adoption with Innovation Ready Software Development and Processor Verification Tools

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New Ecosystem Leads RISC-V Mainstream Adoption with Innovation Ready Software Development and Processor Verification Tools

This title is a lot of words, so let me state this differently:

A processor without an ecosystem is as useful as a
RISC-V History

• RISC-V is an open standard instruction set architecture (ISA) that began in 2010 at the University of California, Berkeley

• Unlike most other ISAs, RISC-V is provided under open source licenses that do not require fees to use
  • This is just the architecture, not the processor implementation

• Unlike other academic designs which are typically optimized only for simplicity of exposition, the designers intended that the RISC-V instruction set be usable for practical computers

• While the ISA is a comprehensive RISC architecture, the RISC-V specification allows for users to add custom features (instructions, CSRs, ...)

• The freedom, and not the free, is why RISC-V usage is growing so fast
Freedom Enables Domain Specific Processing

• RISC-V is growing in market segments where x86 (PCs, data centers) and Arm (mobile) architectures are not dominant
  • Small microcontrollers for SoC management, replacing proprietary cores
  • Verticals such as IoT and automotive
  • Horizontal markets such as security and AI/ML
  • Deep embedded applications

• The freedom of the open ISA enables users to develop differentiated domain specific processors and processing systems

• RISC-V users include traditional semiconductor companies, and embedded systems companies now practicing vertical integration by developing their own SoCs
Motivation for RISC-V Adoption

- Freedom to innovate and differentiate
- PPA = Performance, Power, Area
- No legacy baggage as with other architectures
- Open source => security
- Cost is only a minor factor in choosing RISC-V
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A processor with an ecosystem is a product

OpenHW Group CORE-V MCU Dev Kit
RISC-V Ecosystem
RISC-V Has Learned From Arm

• Arm’s ecosystem came into being somewhat organically, well after devices containing Arm processors were in production

• RISC-V has been building the ecosystem from the beginning, understanding that adoption of RISC-V requires the ecosystem

• Key requirement for ecosystem participants: support the flexibility of RISC-V
  • This could have been an issue, since ecosystem companies like to leverage standard architectures, and customization reduces that leverage
  • However, RISC-V ecosystem companies have developed innovative approaches to support RISC-V customization
Customization & the RISC-V Ecosystem

Customization is not fragmentation

Customization is opportunity

Gold Mining Tools
# The Rich RISC-V Ecosystem

## Applications
- GitHub
- Apache
- PEAKHILLS
- MediaWiki
- MNN
- redis
- MySQL

## Libraries
- OpenSSL
- OpenBLAS
- BLAS
- FFTW
- PyTorch
- WebRTC
- speex
- PerfXLab
- OpenBLAS

## Infrastructure
- SPIKE
- Golden Model
- SAIL

## Runtimes
- AMR
- CSI-NN

## OS
- Hypervisor
- KVM

## Hypervisor
- TinyEMU
- gprof
- openBLAS
- BLIS
- FFTW

## Boot
- TinyEMU
- TinyEMU

## Design Tools + Compilers
- Eclipse
- gprof
- Sparta
- tvm
- GDB
- Green Hills Software
- AR
- codeplay

## Ecosystem Standards, upstream / support common tools
- ISA Extensions, Profiles, Platforms
- Security model, IOMMU, Industry SIGs

## Attributes: Debuggable, Secure, Performant, Reliable/Serviceable/Diagnosable

## Implementation
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*Embedded World 2023*
RISC-V Ecosystem

Hardware
- Processor IP
- Non-processor IP, e.g. NoC, peripherals, ...
- EDA tools for synthesis, simulation, place and route
- DV methodology & verification IP

Software
- Operating systems
- Drivers
- Firmware
- Libraries
- Compilers and tool chains
- Debuggers
- Analysis tools
- Software simulation
RISC-V Hardware Ecosystem Has Two Categories

• ISA-neutral
  • Non-processor IP, e.g. NoC, peripherals, ...
    • Arteris (leader in NoC IP) 2 weeks ago announced collaboration with SiFive
  • EDA tools for synthesis, simulation, place and route, ...
    • All the EDA vendors support RISC-V
    • They do not always talk about that support

• ISA-dependent
  • Processor IP
    • Processor IP vendors
    • Open source collaboration
    • Self-developed processor implementations
  • DV methodology and verification IP
    • The reference model needs to support both the spec and any customization
RISC-V Processor IP Vendors
(small selection of ~30 vendors)
OpenHW Group: Collaboration on Commercial Quality, Open Source, RISC-V Cores

- OpenHW staff and member organizations are working together on processor implementation, verification and software (including tool chains, debugger, OS, ...)

- OpenHW Core-V-Verif
  - OpenHW users now on 3rd generation of Core-V-Verif DV flow
  - CV32E40P successfully taped out
  - CV32E40Pv2, CV32E40S, CV32E40X, CV32E20 using this flow today; all expected to complete DV this year
RISC-V Processor Verification Requires a Flow Supporting Asynchronous Events And Complex Implementations

- Reference model needed for comparison of correct behavior
- Verification IP provides ease of use, saves time and resources
- RVVI standard provides communication between test bench and reference model subsystem
- riscvISACOV: functional coverage modules
- Test suites: riscvISATESTS, directed test suites for difficult extensions

*ImperasDV, with asynchronous continuous compare methodology, is needed to support features such as interrupts, privilege modes, Debug mode, multi-hart, multi-issue and OoO pipeline,...*
RISC-V Software Ecosystem

- Operating systems
- Drivers
- Firmware
- Libraries
- Compilers and tool chains
- Debuggers
- Analysis tools
- Software simulation
The RISC-V Software Ecosystem

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Ecosystem Standards, upstream / support common tools
ISA Extensions, Profiles, Platforms
Security model, IOMMU, Industry SIGs
Architecture Tests
Attributes: Debuggable, Secure, Performant, Reliable/Serviceable/Diagnosable

Implementation
- RTL
- DV

Design & Microarchitecture
- Silicon
- Training
- Research
- Soft IP
- Academia
- Services
Three Ecosystem Success Stories

• OpenHW: CORE-V MCU Dev Kit
• Dolphin Design: “Panther” DSP subsystem IP
• NSITEXE: Data Flow Processor subsystem IP
CORE-V MCU Status

- CORE-V MCU hardware in flight
- CORE-V MCU software simulator (riscvOVPsimCOREV) available today for early software development

- Real Time Operating System (e.g. FreeRTOS) capable ~400+MHz CV32E4 MCU
- Embedded FPGA fabric with hardware accelerators from QuickLogic
- Multiple low power peripheral interfaces (SPI, GPIO, I2C, HyperRAM, CAMIF, etc) for interfacing with sensors, displays, and connectivity modules
- Built in 22FDX with
Ecosystem Collaboration on the SDK (FPGA Prototype)
Dolphin Design: DSP IP with RISC-V

- Dolphin Design develops IP and provides SoC design services
- RISC-V enables product differentiation
- SPEED: System Platforms for Energy Efficient Designs
  - Power management
  - Audio
  - MCU subsystem
  - Neural processing unit
  - “Panther” DSP: high throughput general purpose DSP, with extremely low power consumption
    - 1st generation built with RI5CY open-source RISC-V cores
    - 2nd generation should improve performance, power consumption, quality
    - 2nd generation design choice: OpenHW Group RISC-V core CV32E40Pv2
Panther 2nd Generation Design Choice: OpenHW CV32E40Pv2

- CV32E40Pv1 is an industrial-grade verified core, and has been implemented in SoCs
- CV32E40Pv2 improvements
  - DSP-like capabilities
  - Higher performance
  - Lower power consumption
  - Smaller code size
- CV32E40Pv2 adds
  - Hardware loops
  - Multiply and Accumulate
  - Post-increment load/store
  - 16- and 8-bit SIMD
  - Optional single-precision FPU (RISC-V F extension)
- Can be used as microcontroller, DSP and for neural network applications
NSI-TEXE Has Built IP for AI in Automotive

- 2021-Jul-13: NSITEXE achieves world’s first RISC-V processor with vector extension certified for ISO 26262 ASIL D ready product
- 2021-Aug02: NSITEXE: A New product RISC-V 32bit CPU “NS31A” which supports ISO26262 ASIL D
- 2021-Nov-09: NSITEXE DR1000C, a RISC-V based parallel processor IP with vector extension (DFP: Data Flow Processor) has been licensed for Renesas’ new RH850/U2B Automotive MCUs
Summary

• RISC-V has huge momentum
• Across many markets
• Ecosystem for both hardware and software enables PRODUCT success
Thank you!

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