











Revolutionizing Embedded Software Development

Imperas Newsletter: February 2018

"Silicon without software is just sand."



VIDEOS



New RISC-V Demo Video

See the new video demo of a RISC-V virtual platform, based on RV64GC, booting the Linux kernel, featuring Virtio and our RISC-V EPK with the busybear-linux file system.

Watch it here.

And, view more Imperas videos here.

If you want more information about our RISC-V models, or want to see this platform booting Linux - come and see us at <u>Embedded World.</u>



Embedded World 2018

See Imperas at the Embedded World Exhibition & Conference 2018: February 27 - March 1, at the Nuremberg Exhibition

Centre, Germany. Imperas will demonstrate virtual platforms solutions as part of the RISC-V Foundation booth (3A-419), featuring technology to accelerate embedded software development and test. Imperas will also present two co-authored papers:

- Cycle-Approximate Timing Simulation of RISC-V Processors, by Lee Moore, Duncan Graham and Simon Davidmann, Imperas Software, and Felipe Rosa, Universidad Federal Rio Grande Sud. Presentation: February 27.
- Virtual Platform Environment for the Bring Up and Test of a Secure Many-Core RTOS (Real Time Operating System), authored by Atsushi Shinbo and Shuzo Tanaka of eSOL TRINITY, Masaki Gondo of eSOL, Duncan Graham and Larry Lapides of Imperas Software. Presentation: February 28.

Read more here.



Automotive Testing Expo in Korea

See Imperas virtual platform solutions for automotive software debug, test and verification at the upcoming Automotive Testing Expo, presented by Imperas distribution partner Coontec.

- Where: Booth 2016 at KINTEX in Seoul, Korea.
- When: March 13-15, 2018.

Read more here.

To set up a meeting, please email Imperas at $\underline{sales@imperas.com}$ or Coontec at $\underline{joon@coontec.com}$.

For more information on the show, click here.



RISC-V Conference

Imperas participated and presented high-performance software simulation and virtual platforms at the <u>7th RISC-V Workshop</u>. The Imperas session covers virtual prototypes for software development, debug and test. This

RISC-V Workshop, hosted by Western Digital in Milpitas California November 28-30 2017, brought the RISC-V community together to share information about RISC-V projects underway around the globe, and build consensus on the evolution of the instruction set.

Read more here.

NEWS



Microsemi and Imperas Announce Extendable Platform Kit for Microsemi Mi-V RISC-V Soft CPUs

Microsemi Corporation and Imperas announced the Extendable Platform Kit™ for Microsemi Mi-V™ RISC-V soft central processing units (CPUs). The collaboration delivers the first commercially available instruction set simulator (ISS) for Microsemi's Mi-V ecosystem, a program designed to increase adoption of Microsemi's RISC-V soft CPU product family utilizing RISC-V open instruction set architectures (ISAs).

Read more.



Andes and Imperas Partner to Deliver Models and Virtual Platforms for Andes RISC-V Cores

Imperas provides integrated virtual prototype software solutions and models for Andes RISC-V based architecture AndeStar V5 NX25 and N25 processors.

Read more.

ARTICLES



11 Myths About the RISC-V ISA

New article in Electronic Design, with Imperas. Read it here.



Extendable Platform Kit to Ease Adoption of FPGA-based RISC-V Designs



New article in eeNews Europe by Julien Happich. Read it here.

Big Challenges, Changes For Debug

New article in Semiconductor Engineering by Ann Steffora Mutschler. Read it here.

CASE STUDIES



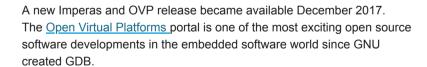
Case Study: NAGRA

NAGRA, a leader in security products for streaming video, is building a new device to protect streaming video in conjunction with a smart TV or set top box. This application program includes hardware (multiple proprietary, many-core SoCs) with supporting software. Their use model is an advanced Agile sprint / Continuous Integration (CI) test methodology, including the Imperas virtual platform, to develop embedded and application software.

Read more.

OVP RELEASE NEWS

OVP: Fast Simulation, Free open source models, Public APIs: Open Virtual Platforms.



Open Virtual Platforms

 For embedded software developers, virtual platforms are increasingly important, especially for multi-core designs.

The resources on this portal can significantly accelerate your development and test. The next release of OVPsim is expected to be available in March, 2018.

Copyright © 2018 Imperas Software Limited, All rights reserved.

<u>Update your preferences</u> or <u>unsubscribe from this list</u>